WHAT IS CLAIMED IS:

1. A turbo decoder for performing decoding using results obtained by decoding a received signal, and subsequently repeating decoding a set number of times using results of decoding obtained successively, comprising:

an error detector for detecting errors in results of decoding in parallel with a decoding operation; and

a controller which, when absence of error has been detected, is operable for outputting results of decoding and halting the decoding operation even if number of times decoding has been performed has not attained said set number of times.

2. A turbo decoder according to claim 1, wherein said controller monitors the number of times errors are detected in decoded results when decoding has been performed said set number of times and executes the decoding operation further if the number of times errors are detected is equal to or less than the set value.

3. A turbo decoder for executing second decoding processing using results of decoding, which are obtained by applying first decoding processing to a received signal, and another received signal, executing the first decoding processing using second results of decoding and said received signal, executing the second decoding processing using first results of decoding and said other received signal, and subsequently executing the first and second decoding processing repeatedly,

comprising:

one elementary decoder for executing said first and second decoding processing;

a selection circuit for selecting, and inputting to the elementary decoder, a prescribed received signal depending upon whether the first or the second decoding processing is executed;

interleaving means for interleaving the first results of decoding;

deinterleaving means for deinterleaving the second results of decoding; and

changeover means for inputting the first and second results of decoding to the elementary decoder via the interleaving means or the deinterleaving means.

4. A turbo decoder for receiving first data, second data obtained by encoding said first data, and third data obtained by interleaving and then encoding said first data, as signals ya, yb and yc, respectively, and executing decoding processing repeatedly using these received signals, comprising:

first and second elementary decoders for executing second decoding processing using results of decoding, which are obtained by applying first decoding processing to prescribed received signals ya, yc, and the other received signal yb, and subsequently executing, repeatedly, first decoding processing using second results of decoding and said received signals ya, yc, and second decoding processing using first results of

decoding and said other received signal yb;

an interleaving unit for interleaving the received signal ya and the second results of decoding and inputting the same to the first elementary decoder together with the received signal yc; and

a deinterleaving unit for deinterleaving the first results of decoding and inputting the same to the second elementary decoder together with the received signal yb;

wherein results of decoding are output from said second elementary decoder.

5. A turbo decoder for receiving first data, second data obtained by encoding said first data, and third data obtained by interleaving and then encoding said first data, as signals ya, yb and yc, respectively, and executing decoding processing repeatedly using these received signals, comprising:

one elementary decoder for executing second decoding processing using results of decoding, which are obtained by applying first decoding processing to a received signal, and another received signal, and subsequently executing, repeatedly, first decoding processing using second results of decoding and said received signal, and second decoding processing using first results of decoding and said other received signal;

an interleaving unit for interleaving the received signal ya and inputting the same to the elementary decoder;

a selection circuit for selecting the signal yc when the first decoding processing is executed, selecting the signal yb when the second decoding processing is executed, and inputting the selected signal to the elementary decoder; and

means for deinterleaving results of the first decoding processing, interleaving results of the second decoding processing and inputting the deinterleaved and interleaved results to the elementary decoder.

6. A turbo decoder for performing decoding using results obtained by decoding a received signal, and subsequently repeating decoding a set number of times using results of decoding obtained successively, comprising:

first and second elementary decoders for executing second decoding processing using results of decoding, which are obtained by applying first decoding processing to a prescribed received signal, and another received signal, and subsequently executing, repeatedly, first decoding processing using second results of decoding and said received signal, and second decoding processing using first results of decoding and said other received signal; and

a selection circuit for selecting and outputting the first and second results of decoding output from said first and second elementary decoders;

wherein the nature of an error generation pattern in decoded data finally output is controlled by

selecting the decoded data to be output.

7. A turbo decoder for performing decoding using results obtained by decoding a received signal, and subsequently repeating decoding a set number of times using results of decoding obtained successively, comprising:

first and second elementary decoders for executing second decoding processing using results of decoding, which are obtained by applying first decoding processing to a received signal, and another received signal, and subsequently executing, repeatedly, first decoding processing using second results of decoding and said received signal, and second decoding processing using first results of decoding and said other received signal; and

a selection circuit for selecting a combination of received signals input to the first elementary decoder that executes said first decoding processing and selecting a received signal input to the second elementary decoder that executes the second decoding processing;

wherein the nature of an error generation pattern in decoded data is controlled by switching the received signals input to the first and second elementary decoders.

8. A turbo decoder for performing decoding using results obtained by decoding a received signal, and subsequently repeating decoding a set number of times

using results of decoding obtained successively, comprising:

one elementary decoder for executing second decoding processing using results of decoding, which are obtained by applying first decoding processing to a received signal, and another received signal, and subsequently executing, repeatedly, first decoding processing using second results of decoding and said received signal, and second decoding processing using first results of decoding and said other received signal; and

a selection circuit for selecting a combination of received signals input to the elementary decoder at a timing at which said first decoding processing is executed, and selecting a received signal input to the elementary decoder at a timing at which said second decoding processing is executed;

wherein the nature of an error generation pattern in decoded data is controlled by switching the received signals input to the elementary decoder at the timings of the first and second decoding processing.